

SFP VOA

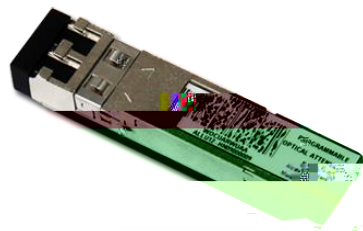


Figure 6: Schematic representation of the proposed model for the generation of the VOA signal. The model involves several components and their interactions:

- The input signal $\ddot{w}$ is processed by a Tap-PD block.
- The output of the Tap-PD block is fed into two parallel paths:
 - A path through a gain block $\hat{A}$ followed by an integrator $\frac{1}{s}$.
 - A path through a gain block $\hat{A}$ followed by a differentiator s .
- The outputs of these two paths are summed at a summing junction.
- The result is then passed through a block labeled I^2C .
- The output of the I^2C block is fed into a block labeled SFP .
- The output of the SFP block is fed into a block labeled $\tilde{U}$.
- The output of the $\tilde{U}$ block is fed into a block labeled MSA .
- The output of the MSA block is fed into a block labeled $\%$.
- The output of the $\%$ block is fed into a block labeled $\neq$.
- The output of the $\neq$ block is fed into a block labeled $\dot{\rho}$.
- The output of the $\dot{\rho}$ block is fed into a block labeled L .
- The output of the L block is fed into a block labeled $\sim$.
- The output of the $\sim$ block is fed into a block labeled $\hat{A}$.
- The output of the $\hat{A}$ block is fed into a block labeled VOA .

SFP	%o
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I ² C	o

$$\begin{array}{ccc} \ddot{\omega} & \tau & \ddot{\omega} w \\ \hline \dot{H} & & \end{array}$$

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Telcordia GR-1221-CORE
RoHS

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